

Customer No.: 31561
Application No.: 10/710,199
Docket NO.: 13875-US-PA-X

AMENDMENT

In the Claims:

Claims 1-13 (cancelled).

Claim 14. (original) A MOS transistor, comprising:

a substrate;

a gate dielectric layer on the substrate;

a stacked gate on the gate dielectric layer, comprising, from bottom to top, a first barrier layer, an interlayer, a work-function-dominating layer, a second barrier layer and a poly-Si layer; and

a source/drain in the substrate beside the gate.

Claim 15.(original) The MOS transistor to claim 14, wherein the interlayer includes a material capable of controlling a crystal orientation of the work-function-dominating layer to adjust a work function of the work-function-dominating layer.

Claim 16.(original) The MOS transistor according to claim 14, wherein the interlayer includes a material capable of wetting a surface of the first barrier layer.

Claim 17.(original) The MOS transistor according to claim 14, wherein a thickness of the interlayer is smaller than a thickness of the work-function-dominating layer.

Claim 18.(original) The MOS transistor according to claim 14, wherein a thickness of the work-function-dominating layer is larger than a total thickness of the first and second barrier layers.

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Claim 19.(original) The MOS transistor according to claim 14, wherein the gate dielectric layer comprises a high-K dielectric layer.

Claim 20.(original) The MOS transistor according to claim 14, further comprising:

a spacer on a sidewall of the gate; and

a pair of lightly doped drains in the substrate,

wherein the source/drain is in the substrate beside the spacer, and the lightly doped drains are in the substrate beside the gate connecting with the source/drain.